Course Title	RTL Modeling with System Verilog for Simulation and Synthesis				Course Type		Integrated	
Course Code	M22TM0301	Credits	4		Class		I Semester	
RTL Simulation and Synthesis	TLP	Credits	Contact Hours	Work Load	Total Number of Classes Per Semester		Assessment in Weightage	
	Theory	3	3	3				
	Practice	1	2	2				
	-	-	-	-	Theory	Practical	IA	SEE
	Total	4	5	5	**39**	**26**	**50 %**	**50 %**

COURSE OVERVIEW:

Verilog has been extended and matured into the system Verilog langiage of today, and includes major new abstact constructs, test-bench verification, formal analysis. System Verilog adds powerful language constructs for modeling and verifying the behavior of designs that are ever increasing in size and complexity. This course focuses on using system Verilog for modeling digital ASIC and FPGA designs at the RTL level of abstraction. The course initially introduces system Verilog as its starting point.

COURSE OBJECTIVES:

The objectives of this course are:

1. To present a brief overview of simulating and synthesizing the system Verilog
2. To provide an overview of RTL modeling in system Verilog
3. To understand the system Verilog language constructs
4. To study combinational and sequential modiling using system Verilog
5. To model the latches in RTL Models

COURSE OUTCOMES(COs)

On successful completion of this course; the student shall be able to:

CO#	Course Outcomes	POs	PSOs
CO1	Explore the simulation and synthesis of system Verilog	1,2,3,4	1,2,3
CO2	Illustrate the overview of RTL Modeling in system Verilog	1,2,3,4,5	1,2,3
CO3	Introduce the system Verilog language constructs	1,2,3,4	1,2,3
CO4	Use of programing statements in System Verilog with an emphasis on proper RTL coding guidelines in order to ensure the code will synthesize to the gate level implementation inteded	1,2,3,4,5	1,2,3
CO5	Developing RTL Models of combinational logic and sequential logic	1,2,3,4,5	1,2,3
Co6	Model and handle latches in RTL models and how to avoid unintentional latches	1,2,3,4,5,7,8, 9,11	1,2,3

BLOOM'S LEVEL OF THE COURSE OUTCOMES

CO#	Bloom's Level					
	Remember (L1)	Understand (L2)	Apply (L3)	Analyze (L4)	Evaluate (L5)	Create (L6)
CO1	✓	✓	✓			
CO2	✓	✓	✓	✓		
CO3	✓	✓	✓	✓		
CO4	✓	✓	✓	✓	✓	
CO5	✓	✓	✓	✓	✓	
CO6	✓	✓	✓			

COURSE ARTICULATION MATRIX

CO#/ Pos	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	3	3								2	1	2
CO2	3	3	2	2	2							2	1	2
CO3	3	3	3	2								2	1	2
CO4	3	2	2	1	2							2	1	2
CO5	3	2	2	1	2							2	1	2
CO6	3	2	2	1							2	3	2	1

Note:1-Low,2-Medium,3-High

COURSE CONTENT
THEORY:

Contents

UNIT - 1

System Verilog Simulation and Synthesis: Verilog and System Verilog – Brief History, RTL and gate level modeling, Defining an RTL synthesis subset of system Verilog, Modeling for ASICs and FPGAs, System Verilog simulation, Digital Synthesis, System Verilog lint checkers

RTL Modeling Fundamentals: Modules and procedural blocks, System Verilog language rules,Modules, modules instances and hierarchy, Net and vairables types,Four state data values, literal values, types and data types, variable types,net types, port declarations,unpacked arrays of nets and variables, parameter constants, const variables, User defined types and packages, user defined types, system Verilog packages, the $unit declaration space, enumerated types, structures, Unions.

UNIT - 2
RTL expression operators: Operator expression rules, concatenate and replicate operators, conditional operator, bitwise operators, reduction operators, logical operators, comparision operators, case equality, set membership, shift operators, streaming operators, arithmetic operators, increment and decrement operators, cast operators and type conversions, operator precedence, system Verilog procedural blocks, decision statements, loopong statements,Jump statements, No-op statements, Functions and tasks in RTL modeling
UNIT - 3
Modeling Combinational Logic: Continuous assignments, the always and always_comb procedures,using functions to represent combinational logic, combinational logic decision priority Modeling sequential logic: RTL Models of filp-flops and registers, modeling FSM, modeling memory devices
UNIT -4
Modeling latches and avoiding unintentional latches: Modeling latches, Uniintentional latch inference, Avoiding latches in intentinally incomplete decisions **Modeling Communication Buses- Interface ports:** Interface port concepts, Using interfaces as module ports, interface mod ports, interfacing methods, interfacing procedural code

Text Books:

1. Stuart Sutherland, RTL Modeling with SystemVerilog for Simulation and Synthesis Using SystemVerilog for ASIC and FPGA Desig.
2. Richard S. Sandige, Modern Digital Design , MGH, International Editions
3. T.R. Padmanabhan, B. Bala Tripura Sundari , Design through Verilog HDL", Wiley Publication.
4. Pong P Chu, "FPGA Prototyping by Verilog Examples", Wiley.

Reference Books:

1. Frank Vahid, "Digital Design", Wiley, 2006.
2. Palnitkar, Samir. Verilog HDL: a guide to digital design and synthesis . Pearson Education India, 2003.

PRACTICE SESSION:

Sl. No.	Name of the Practice Session	Tools and Techniques	Expected Skill /Ability
1	Write a program to demonstrate two-state and four-state data types.	Appropriate EDA Tool	System Verilog programing
2	Write a program to demonstrate push_front, pop_front, push_back and pop_back with respect to Queues.	Appropriate EDA Tool	System Verilog programing
3	Declare four variables red, black, white and green through Enumerated type declaration, use the keywords 'first' and 'next' to step through the variables and display the output.	Appropriate EDA Tool	System Verilog programing
4	Demonstrate Full adder with 'Interface' construct.	Appropriate EDA Tool	System Verilog programing
5	Write a program to demonstrate the difference between 'rand' and	Appropriate	System

	'randc'	EDA Tool	Verilog programing
6	Demonstrate Random Control with randcase and $urandom_range.	Appropriate EDA Tool	System Verilog programing
7	Demonstrate 4-bit adder with the verification environment.	Appropriate EDA Tool	System Verilog programing
8	Demostrate modeling and handling latches RTL design	Appropriate EDA Tool	System Verilog programing
9	Design a UART using system Verilog a. Design Transmitter logic. b. Design Receiver logic. c. Design a top level test bench	Appropriate EDA Tool	System Verilog programing

Text Books:

5. Stuart Sutherland, RTL Modeling with SystemVerilog for Simulation and Synthesis Using SystemVerilog for ASIC and FPGA Design, 2017.
6. Richard S. Sandige, Modern Digital Design , MGH, International Editions
7. T.R. Padmanabhan, B. Bala Tripura Sundari , Design through Verilog HDL", Wiley Publication.
8. Pong P Chu, "FPGA Prototyping by Verilog Examples", Wiley, 2006.

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